



PRESS RELEASE

TransEDA announces the first production release of Assertain™

Los Gatos, CA and Eastleigh, UK - January 30th, 2006 - TransEDA, the leader in Coverage and Verification Measurement solutions for electronic designs, today announces the availability of **Assertain** production release, the next generation verification closure solution that delivers, in a single environment, total measurement and control of the digital design verification process.

Assertain seamlessly integrates rule, protocol and assertion checking; code and assertion coverage; design and assertion coverability analysis; test suite optimization and specification coverage using proven requirements traceability techniques.

Covering all front-end stages from original text specification through to validated RTL, **Assertain** monitors the verification process, providing engineers with all necessary data to better control design verification, thereby enabling a faster convergence toward sign-off coverage criteria.

Assertain has been extensively tested to be ready for production release at EDSF in Yokohama, Japan, where the tool will be demonstrated.

Assertain packaging

To match the designers' and verification engineers' needs, **Assertain** is available in three different levels that correspond to different types of application:

Assertain HDL quantifies the dynamic verification of pure RTL designs that do not make use of any assertions. It encompasses all functionalities of TransEDA's best selling Verification Navigator suite (extensive rule checking and comprehensive code and FSM coverage with test suite optimization capabilities) with additional SystemVerilog support. Assertain HDL is fully backward compatible with Verification Navigator scripts and files, enabling the smoothest possible transition from one product line to the other.

Assertain ABV has been designed to closely manage assertion-based verification flows by using TransEDA's unique assertion coverage metrics. This package includes all Assertain HDL features, and extends them with advanced rule checking, design coverability analysis and dynamic assertion coverage measurement. Assertain ABV allows engineers to get the most complete and accurate view of how well their tests exercise both the RTL code and the assertions. This completeness is brought by TransEDA's unparalleled set of coverage metrics, among which the newly introduced assertion step and variable coverage metrics. Accuracy is achieved by running coverability analysis on the design to filter all unreachable code branches and expression terms from the final coverage results. In addition, extended rule checking with automatic formal checks is performed when loading a design into Assertain to filter most simple bugs prior to simulation.

Assertain VCM is the most complete version of the product, enabling a total control of the validation and verification process, from text specification to validated RTL design. The VCM level augments Assertain ABV functionalities with coverability analysis on the assertions, proven formal assertion checking capabilities and unique specification coverage metrics. Assertain VCM enables the effective implementation of a complete specification-to-closure verification flow under full user control.

Migration program for Verification Navigator™ customers

TransEDA has started an attractive migration program for the current customers of any of the Verification Navigator tools VN-Check, VN-Cover or VN-Optimize. Many customers under maintenance have already committed to transition to **Assertain**. Other Verification Navigator customers will be able to migrate at their maintenance renewal time or at their earliest convenience. For more information about the **Assertain** migration program, customers may contact their local TransEDA representative or email migration@transeda.com.

“After many presentations done at numerous customer sites, I am glad to see the high interest Assertain has generated in the verification community. This explains why so many customers have trusted us and committed to migrate to a new product which was not yet in production” said Jean-Luc Bouvresse, CEO of TransEDA. “Now that we have released Assertain on schedule, we are able to fulfill our commitments and deliver what our customers expected.”

Pricing and Availability

Assertain HDL and **ABV** are available now on Solaris and Linux platforms for VHDL, Verilog and SystemVerilog languages. PSL assertions support will be added at the end of February. Pricing starts from \$16K for an annual subscription license of Assertain HDL.

For more information about the Assertain product line, contact your local TransEDA representative or email info@transeda.com.

About TransEDA

TransEDA is a leading provider of coverage and verification measurement solutions for electronic designs.

The company markets an advanced Verification Closure Measurement environment that takes advantage of both static and dynamic technologies to give engineers access to a unified view of their design verification progress.

Unique functionalities such as comprehensive assertion coverage, coverability analysis, specification coverage with engineering change impact analysis, and automatic bus protocol checking, enhance traditional code coverage, test suite optimization, HDL rule checking and static assertion checking capabilities to form an integrated Verification Closure Management solution. Other products include verification IP with bus-based system-level test automation and transistor-level functional abstraction.

TransEDA has offices in North America, Europe and Japan, plus local representatives in China, India, Korea, Singapore and Taiwan. For more information, visit www.transeda.com.

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