



PRESS RELEASE

TransEDA announces PSL support in Assertain™

Los Gatos, CA and Eastleigh, UK - March 2nd, 2006 - TransEDA, the leader in Verification Closure Measurement solutions for electronic designs, today announces the availability of PSL language in Assertain, the innovative verification closure solution that delivers, in a single environment, total measurement and control of the digital design verification process.

Recently released with support for VHDL, Verilog and SystemVerilog designs and SystemVerilog Assertions (SVA), Assertain has been extended to now accept PSL assertions as well, in both VHDL and Verilog flavors.

Covering all front-end stages from original text specification through to validated RTL, Assertain helps manage the verification process, providing engineers with all necessary data to better control design verification, thereby enabling faster convergence toward sign-off coverage criteria.

Assertain seamlessly integrates rule, protocol and assertion checking; code and assertion coverage; design and assertion coverability analysis; test suite optimization and specification coverage using proven requirements traceability techniques.

Assertion coverage benefits

Including unique step and variable assertion coverage metrics, Assertain provides detailed coverage information on both SVA and PSL assertions with an accuracy that goes far beyond the basic pass/fail indication displayed by most simulators.

In this way Assertain enables precise measurements of how well assertions have been exercised by the test benches and how well they cover the RTL behavior they represent. Users can therefore get the greatest return on investment for the time spent writing and tuning assertions.

The cross-linked results from assertion, functional, code and FSM coverage are combined in a single, unified database that provides a clear view of how design verification is progressing.

Tool availability

Assertain is available now on Solaris and Linux platforms for VHDL, Verilog and SystemVerilog designs. Assertions can be expressed in PSL or in SVA.

For more information about the Assertain product line, contact your local TransEDA representative or email info@transeda.com.

About TransEDA

TransEDA is the leader in Verification Closure Measurement solutions for electronic designs.

The company markets an advanced verification closure environment that takes advantage of both static and dynamic technologies to give engineers access to a unified view of their design verification progress.

Unique functionalities such as detailed assertion coverage, coverability analysis, specification coverage with impact analysis and automatic bus protocol checking, enhance traditional coverage and verification technologies to form an integrated Verification Closure Measurement solution.

TransEDA has offices in North America, Europe and Japan, plus local representatives in China, India, Korea, Singapore and Taiwan. For more information, visit www.transeda.com.

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